10577"6020001

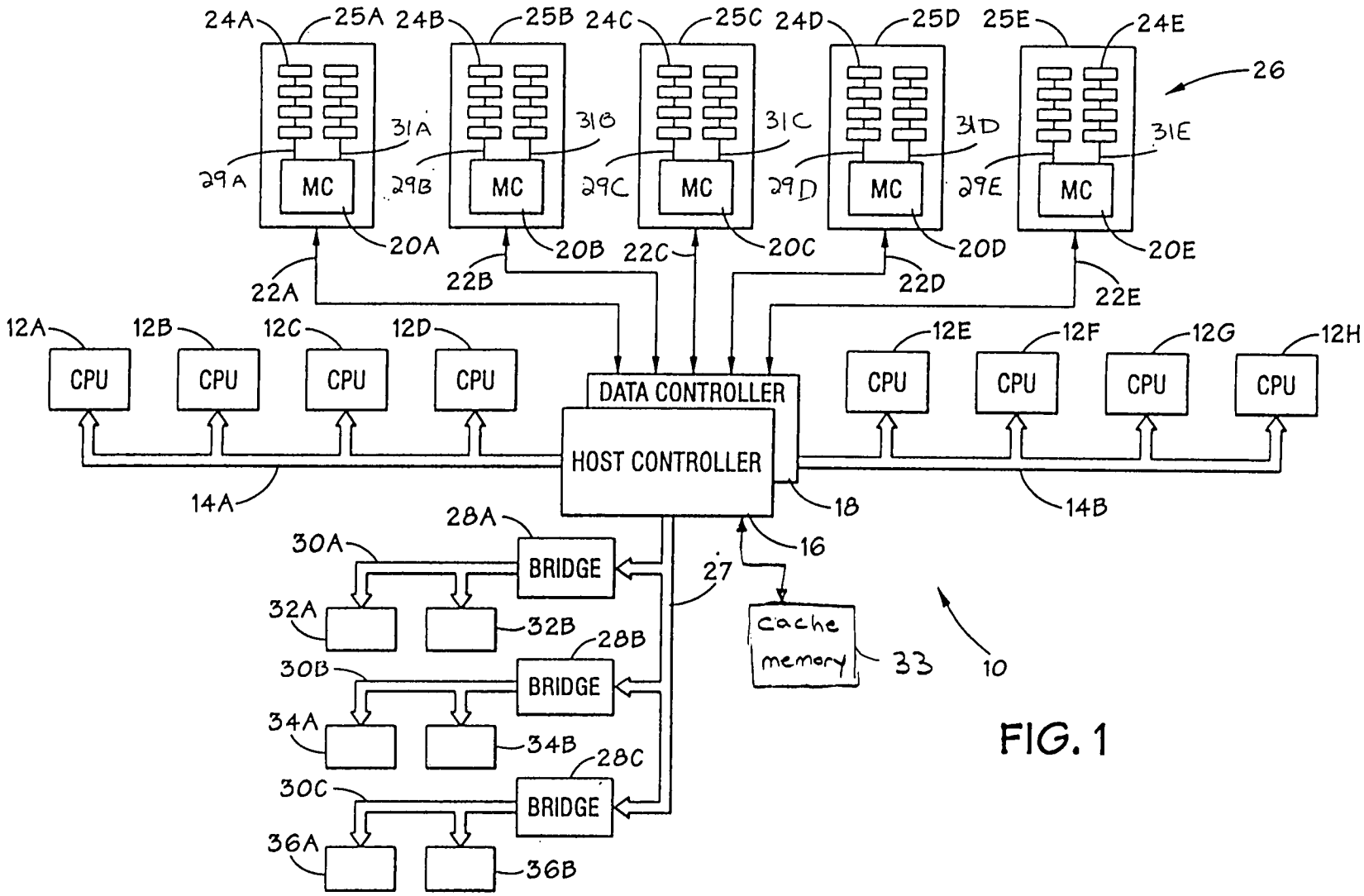

FIG. 1

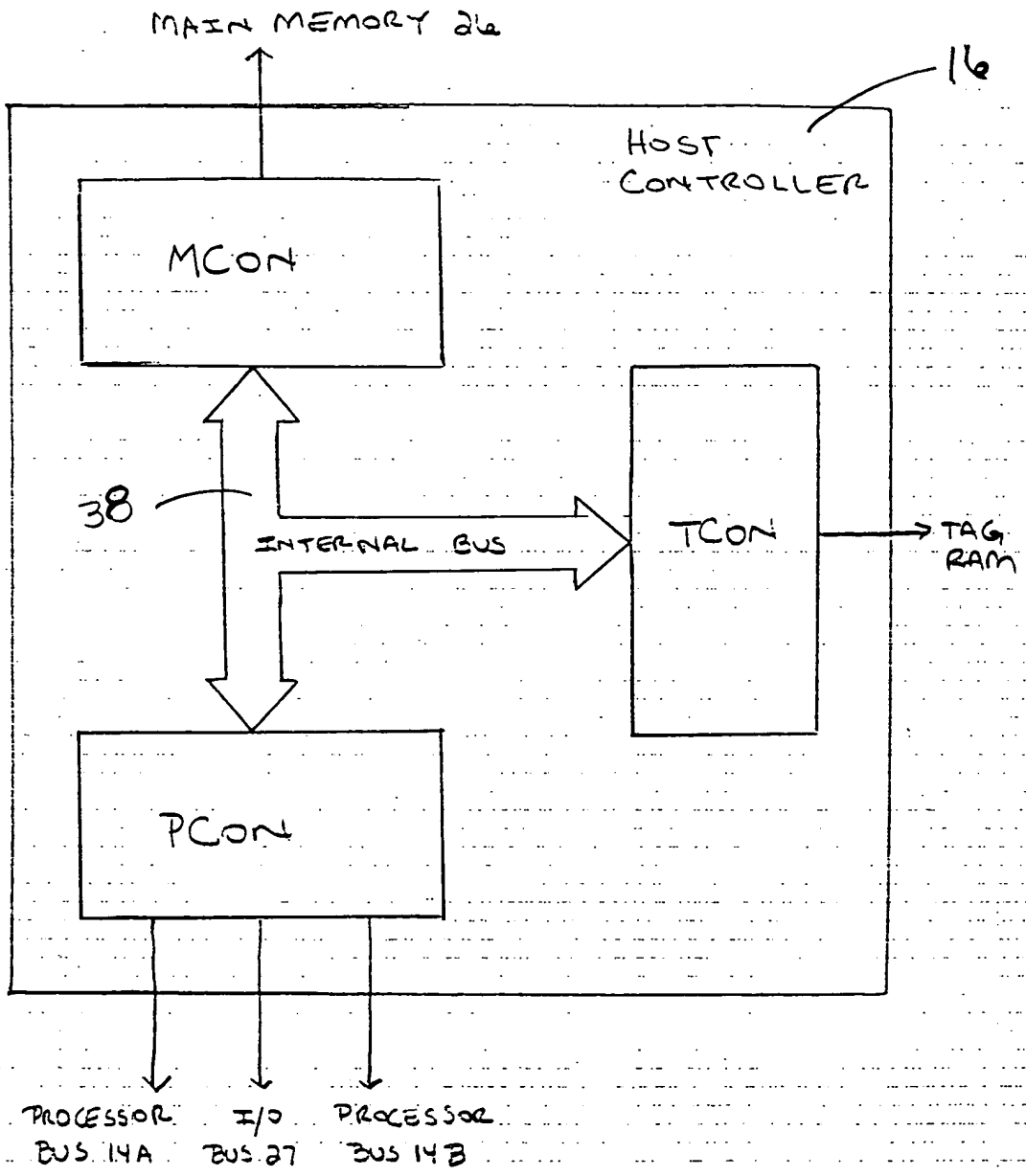
MAIN MEMORY 26
16
HOST CONTROLLER
MCON
38
INTERNAL BUS
TCON
TAG RAM
PCON
PROCESSOR BUS 14A
I/O BUS 27
PROCESSOR BUS 14B

Fig. 2

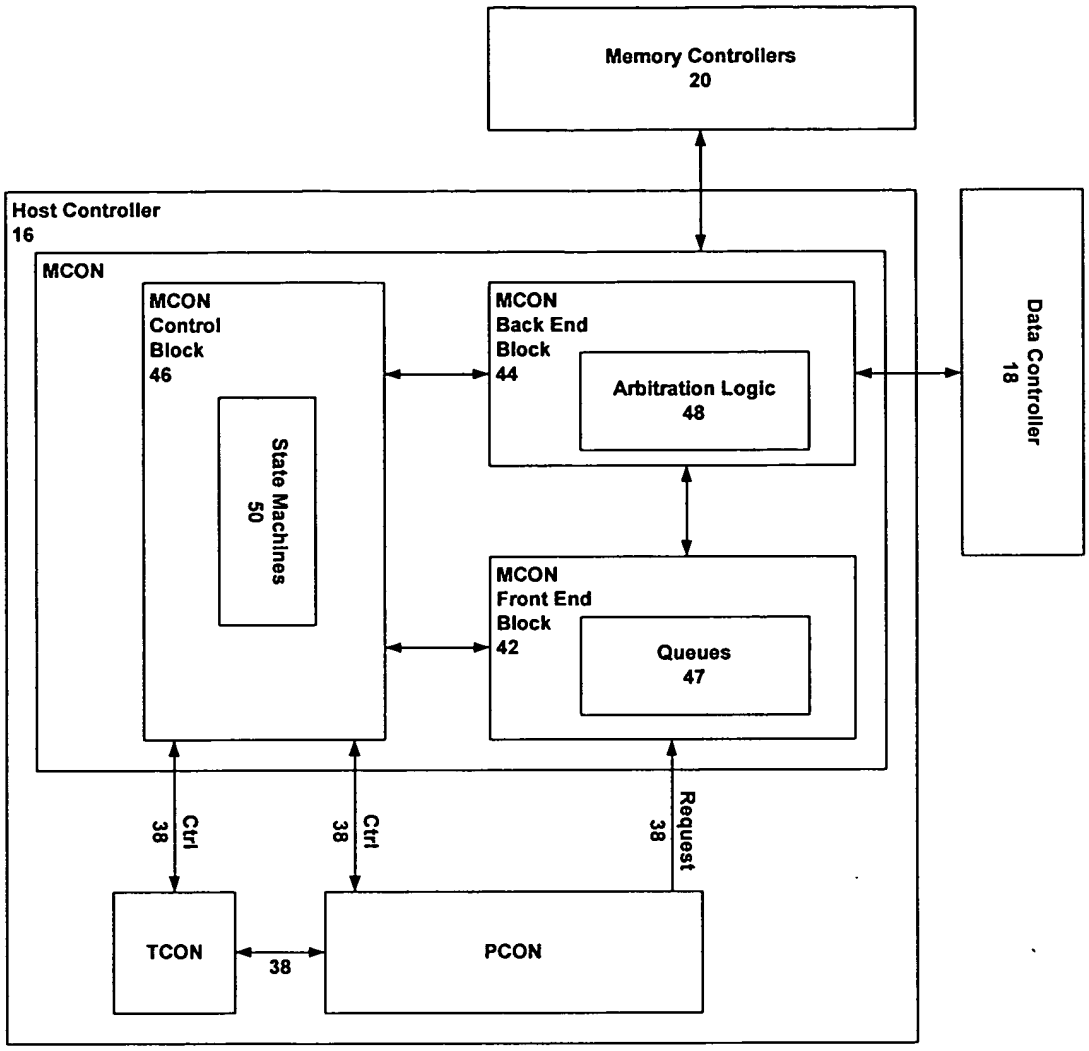
Memory Controllers
20
Host Controller
16
MCON
MCON
Control
Block
46
State Machines
50
MCON
Back End
Block
44
Arbitration Logic
48
MCON
Front End
Block
42
Queues
47
Data Controller
18
38
Ctrl
38
Ctrl
38
Request
TCON
38
PCON

Figure 3

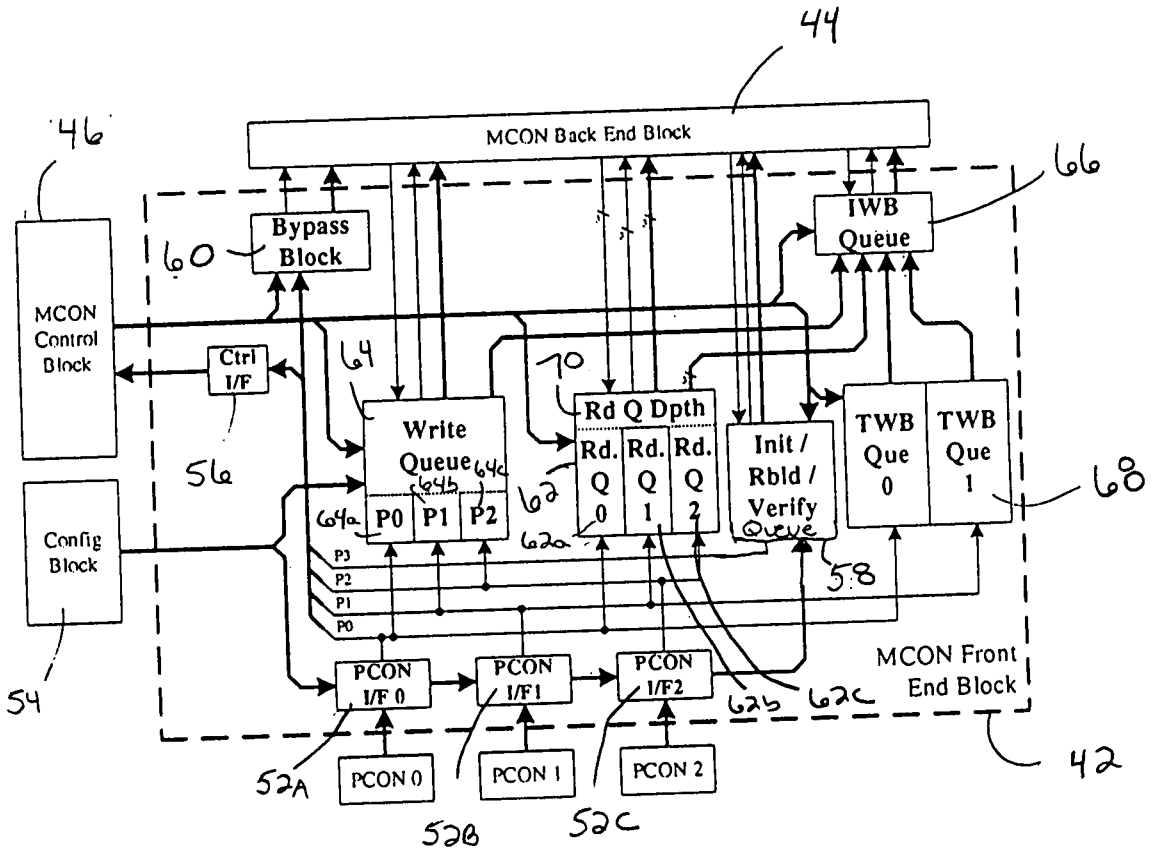
44
MCON Back End Block
46
66
Bypass Block
60
IWB Queue
MCON Control Block
Ctrl I/F
64
70
Rd Q Dpth
Write Queue
Rd. Q 0
Rd. Q 1
Rd. Q 2
Init / Rbld / Verify Queue
TWB Que 0
TWB Que 1
68
56a
64b
64c
64a
P0
P1
P2
62
62a
Config Block
P3
P2
P1
P0
58
54
PCON I/F 0
PCON I/F1
PCON I/F2
MCON Front End Block
62b
62c
42
52A
PCON 0
PCON 1
PCON 2
52B
52C

Fig. 4

T05TTT"6082000T

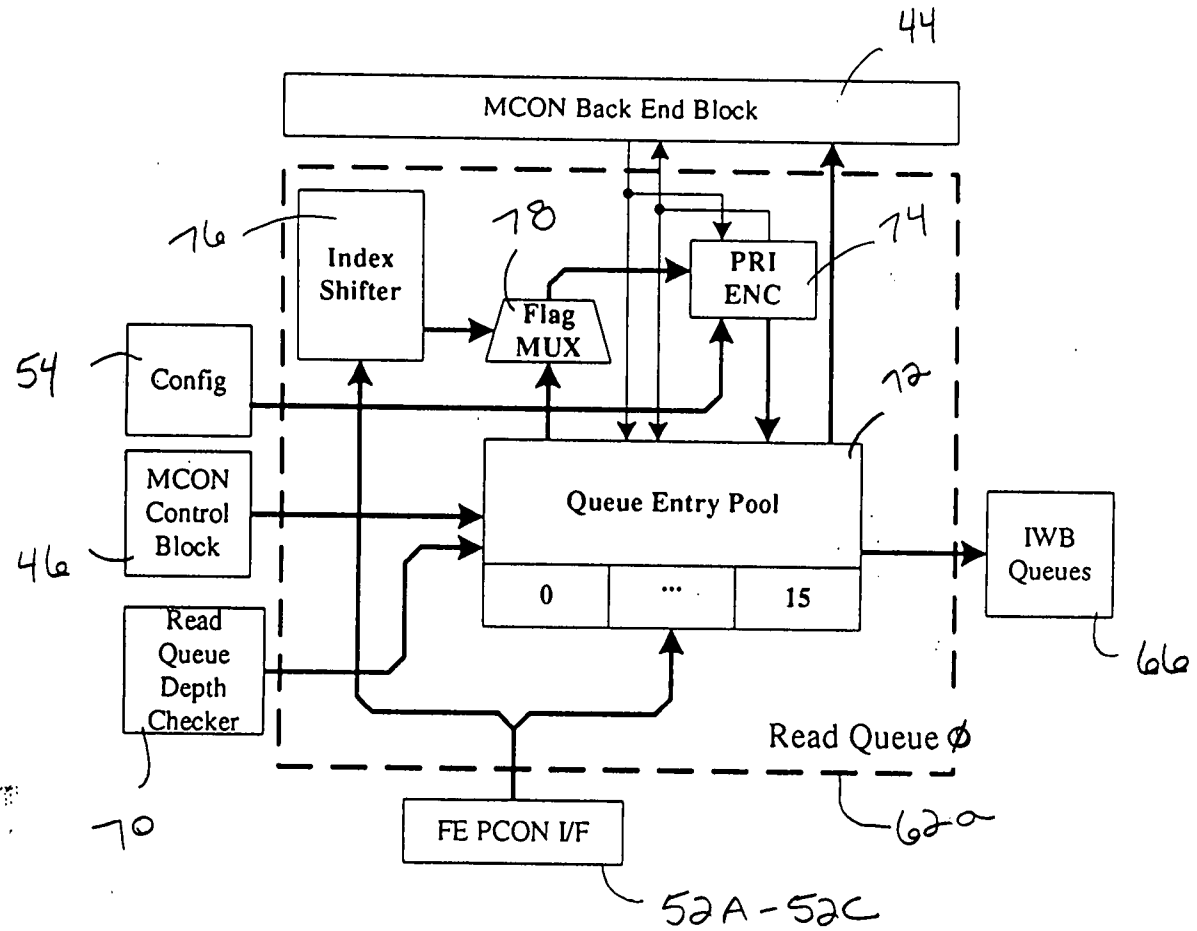

Fig. 5

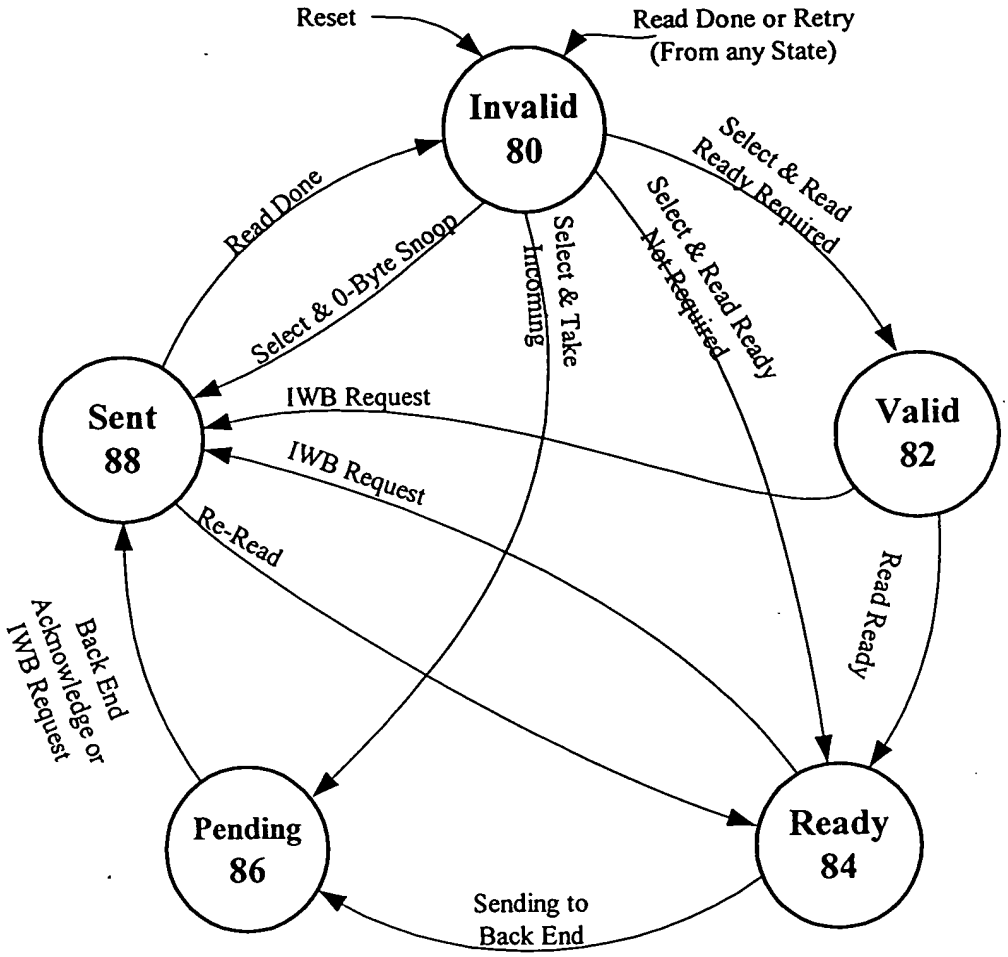
Reset
Read Done or Retry
(From any State)
Invalid
80
Select & Read
Ready Required
Read Done
Select & 0-Byte Snoop
Select & Take
Incoming
Select & Read Ready
Not Required
Sent
88
Valid
82
IWB Request
IWB Request
Re-Read
Read Ready
Back End
Acknowledge or
IWB Request
Pending
86
Ready
84
Sending to
Back End

Figure 6

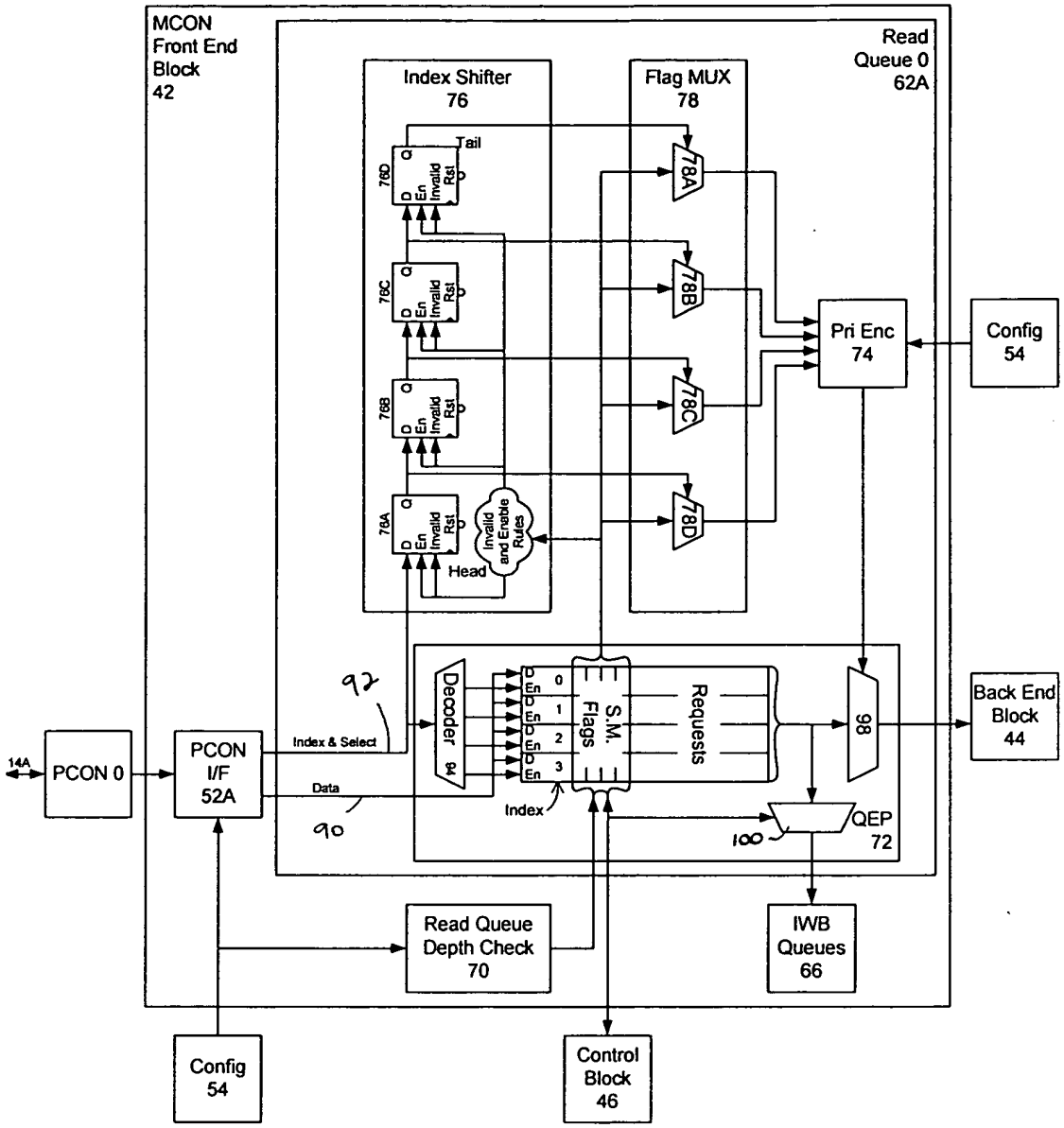
MCON
Front End
Block
42
Read
Queue 0
62A
Index Shifter
76
Flag MUX
78
Tail
Head
Invalid and Enable Rules
Pri Enc
74
Config
54
Back End
Block
44
PCON 0
14A
PCON
I/F
52A
Index & Select
Data
92
90
Decoder
3x8
S.M.
Flags
Requests
98
Index
QEP
72
100
Read Queue
Depth Check
70
IWB
Queues
66
Config
54
Control
Block
46

Figure 7